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AF/2859

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
Application Number	10/099,641
Filing Date	March 15, 2002
First Named Inventor	Wilbur G. Catabay et al.
Examiner Name	Lisa A. Kilday
Art Unit	2829
Attorney Docket No.	99-102/1D

METHOD OF PAYMENT *(check all that apply)*

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1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below		Fee Paid
Total Claims		-20**=		x =	
Independent Claims		- 3** =		x =	
Multiple Dependent				=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330

SUBMITTED BY				(Complete *(if applicable)*)	
Name (Print/Type)	John P. Taylor	Registration No. (Attorney/Agent)	22,369	Telephone	(909) 303-1416
Signature	John P. Taylor			Date	24-FEB-2004

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Practitioner's Docket No. 99-102/1D **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Wilbur G. Catabay and Richard Schinella
Application No.: 10 / 099,641 Group No.: 2829
Filed: March 15, 2002 Examiner: Lisa A. Kilday
For: LOW K DIELECTRIC COMPOSITE LAYER FOR INTEGRATED CIRCUIT STRUCTURE WHICH PROVIDES VOID-FREE LOW K DIELECTRIC MATERIAL BETWEEN METAL LINES WHILE MITIGATING VIA POISONING

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Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION—37 C.F.R. § 1.192)

NOTE: The phrase "the date on which" an "appeal was taken" in 35 U.S.C. 154(b)(1)(A)(ii) (which provides an adjustment of patent term if there is a delay on the part of the Office to respond within 4 months after an "appeal was taken") means the date on which an appeal brief under § 1.192 (and not a notice of appeal) was filed. Compliance with § 1.192 requires that: 1. the appeal brief fee (§ 1.17(c)) be paid (§ 1.192(a)); and 2.the appeal brief complies with § 1.192(c)(1) through (c)(9). See Notice of September 18, 2000, 65 Fed. Reg. 56366, 56385-56387 (Comment 38).

1. Transmitted herewith, in triplicate, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal filed on January 14, 2004.

NOTE: "Appellant must, within two months from the date of the notice of appeal under § 1.191 or within the time allowed for reply to the action from which the appeal was taken, if such time is later, file a brief in triplicate. . . " 37 C.F.R. § 1.192(a) (emphasis added).

CERTIFICATION UNDER 37 C.F.R. §§ 1.8(a) and 1.10*
*(When using Express Mail, the Express Mail label number is **mandatory**; Express Mail certification is optional.)*

I hereby certify that, on the date shown below, this correspondence is being:

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37 C.F.R. § 1.8(a)

☒ with sufficient postage as first class mail.

37 C.F.R. § 1.10 *

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TRANSMISSION

☐ facsimile transmitted to the Patent and Trademark Office, (703) _____-_____.

John P. Taylor
Signature

Date: February 24, 2004

John P. Taylor
(type or print name of person certifying)

** Only the date of filing (§ 1.6) will be the date used in a patent term adjustment calculation, although the date on any certificate of mailing or transmission under § 1.8 continues to be taken into account in determining timeliness. See § 1.703(f). Consider "Express Mail Post Office to Addressee" (§ 1.10) or facsimile transmission (§ 1.6(d)) for the reply to be accorded the earliest possible filing date for patent term adjustment calculations.*

2. STATUS OF APPLICANT

This application is on behalf of

☒ other than a small entity.

☐ a small entity.

A statement:

☐ is attached.

☐ was already filed.

3. FEE FOR FILING APPEAL BRIEF

Pursuant to 37 C.F.R. § 1.17(c), the fee for filing the Appeal Brief is:

☐ small entity	$165.00
☒ other than a small entity	$330.00

Appeal Brief fee due $ 330.00

4. EXTENSION OF TERM

NOTE: 37 C.F.R. § 1.704(b) ". . .an applicant shall be deemed to have failed to engage in reasonable efforts to conclude processing or examination of an application for the cumulative total of any periods of time in excess of three months that are taken to reply to any notice or action by the Office making any rejection, objection, argument, or other request, measuring such three-month period from the date the notice or action was mailed or given to the applicant, in which case the period of adjustment set forth in § 1.703 shall be reduced by the number of days, if any, beginning on the day after the date that is three months after the date of mailing or transmission of the Office communication notifying the applicant of the rejection, objection, argument, or other request and ending on the date the reply was filed. The period, or shortened statutory period, for reply that is set in the Office action or notice has no effect on the three-month period set forth in this paragraph."

NOTE: The time periods set forth in 37 C.F.R. § 1.192(a) are subject to the provision of § 1.136 for patent applications. 37 C.F.R. § 1.191(d). See also Notice of November 5, 1985 (1060 O.G. 27).

NOTE: As the two-month period set in § 1.192(a) for filing an appeal brief is not subject to the six-month maximum period specified in 35 U.S.C. § 133, the period for filing an appeal brief may be extended up to seven months. 62 Fed. Reg. 53,131, at 53,156; 1203 O.G. 63, at 84 (Oct. 10, 1997).

The proceedings herein are for a patent application and the provisions of 37 C.F.R. § 1.136 apply.

(complete (a) or (b), as applicable)

(a) ☐ Applicant petitions for an extension of time under 37 C.F.R. § 1.136 (fees: 37 C.F.R. § 1.17(a)(1)-(5)) for the total number of months checked below:

Extension (months)	Fee for other than small entity	Fee for small entity
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☐ three months	$ 950.00	$ 475.00
☐ four months	$ 1,480.00	$ 740.00
☐ five months	$ 2,010.00	$ 1,005.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request $_____

or

(b) ☒ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal brief fee $ 330.00

Extension fee (if any) $_____

TOTAL FEE DUE $ 330.00

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A duplicate of this paper is attached.

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NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to change the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, *1065 O.G. 31-33.*

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AND/OR

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Date: February 24, 2004

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SIGNATURE OF PRACTITIONER

John P. Taylor

(type or print name of practitioner)

c/o Sandeep Jaggi,
Chief Intellectual Property Counsel

P.O. Address

LSI Logic Corporation
Legal Department - IP
1621 Barber Lane, MS D-106
Milpitas, CA 95035

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

Appellants:	Wilbur G. Catabay and Richard Schinella
Serial Number:	10/099,641
Filed::	March 15, 2002
For:	LOW K DIELECTRIC COMPOSITE LAYER FOR INTEGRATED CIRCUIT STRUCTURE WHICH PROVIDES VOID-FREE LOW K DIELECTRIC MATERIAL BETWEEN METAL LINES WHILE MITIGATING VIA POISONING
Group Art Unit:	2829
Examiner:	Lisa A. Kilday
Docket No.:	99-102/1D
Notice of Appeal Filed::	January 14, 2004
Appeal No.	Not Known

******

BRIEF ON APPEAL

February 24, 2004

This brief is submitted in triplicate as an appeal from the Final Rejection of Appellants' claims mailed July 16, 2003. Final Rejection of claims 15-19 is hereby appealed. No oral hearing is requested.

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(1) REAL PARTY IN INTEREST

LSI Logic Corporation of Milpitas, CA, is the assignee of the entire right, title and interest in and to the invention claimed in this patent application, and thereby is the real party in interest.

(2) RELATED APPEALS AND INTERFERENCES

Applicant's undersigned attorney is not aware of any related appeals and/or interferences now or previously pending before the United States Patent and Trademark Office.

(3) STATUS OF CLAIMS

Claim 1-14	Cancelled in Preliminary Amendment dated March 15, 2002.
Claim 15	Original Claim, Rejected under 35 U.S.C. 102 (b).
Claim 16	Original Claim, Rejected under 35 U.S.C. 102 (b).
Claim 17	Original Claim, Rejected under 35 U.S.C. 102 (b).
Claim 18	Added in Preliminary Amendment dated March 15, 2002, Rejected under 35 U.S.C. 102 (b).
Claim 19	Added in Preliminary Amendment dated March 15, 2002. Rejected under 35 U.S.C. 102 (b).

(4) STATUS OF AMENDMENTS

Preliminary Amendment mailed March 15, 2002,
Status: Entered.

Amendment dated April 2, 2003
(Response to January 31, 20003 Rejection)
Status: Entered

Amendment dated September 16, 2003
(Response to July 16, 2003 Final Rejection)
Status: Entry Refused.

Note that Appellants' response to the Final Rejection was refused entry despite the fact that the Examiner cited a new reference in her Final Rejection even though Appellants' claims were not amended subsequent to the first Office Action.

(5) SUMMARY OF THE INVENTION

(i) Summary in Paragraph Form with Numerals Referring to Drawings

A composite layer of low k silicon oxide dielectric material is formed on an oxide layer 10 of an integrated circuit structure 2. The composite layer of low k silicon oxide dielectric material exhibits void-free deposition properties in high aspect ratio regions, deposition rates in other regions comparable to standard k silicon oxide, and without exhibiting via poisoning characteristics.

The composite layer of low k silicon oxide dielectric material comprises a first layer 24 of low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions, deposited until said low k silicon oxide dielectric material reaches the level of the top of metal lines 14a-14c on oxide layer 10.

A second layer 30 of low k silicon oxide dielectric material is deposited over first layer 24 at a faster rate than the deposition rate of first layer 24 up to the desired overall thickness of the composite layer of low k carbon-doped silicon oxide dielectric material.

The first layer of low k silicon oxide dielectric material may comprise a low k carbon-doped silicon oxide dielectric material formed by reacting a carbon-substituted silane reactant with hydrogen peroxide until the resulting deposition of low k carbon-substituted silicon oxide dielectric material reactant product reaches the level of the top of metal lines 14a-14c on oxide layer 10.

The second layer of low k silicon oxide dielectric material may comprise a layer of low k carbon-doped silicon oxide dielectric material formed over the first layer by plasma enhanced chemical vapor deposition (PECVD) up to the desired overall thickness of the low k carbon-doped silicon oxide dielectric layer.

(ii) Summary in Side by Side Comparison Form with Text in Specification to Show Support for Summary

A composite layer of low k silicon oxide dielectric material is formed on an oxide layer 10 of an integrated circuit structure 2.	"...a composite layer of low k silicon oxide dielectric material is formed on an oxide layer of an integrated circuit structure on a semiconductor substrate..." Page 4, lines 28-29. (See also page 6, lines 10-11; and page 7, lines 3-6)
The composite layer of low k silicon oxide dielectric material exhibits void-free deposition properties in high aspect ratio regions, deposition rates in other regions comparable to standard k silicon oxide, and without exhibiting via poisoning characteristics.	"...a composite layer of low k silicon oxide dielectric material wherein the portion of the composite low k layer of silicon oxide dielectric material deposited in the high aspect ratio regions between the closely spaced apart metal lines is void-free, while the second portion of the composite low k layer of silicon oxide dielectric material deposited above the first portion can be deposited at a much greater deposition rate, yet does not appear to contribute to poisoning of vias formed through the composite layer." Page 13, lines 20-25
The composite layer of low k silicon oxide dielectric material comprises a first layer 24 of low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions, deposited until said low k silicon oxide dielectric material reaches the level of the top of metal lines 14a-14c on oxide layer 10.	"...depositing over the oxide layer and the metal lines a first layer of a low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions between closely spaced apart metal lines until the resulting deposition of low k silicon oxide dielectric material reaches the level of the top of the metal lines on the oxide layer." Page 6, lines 15-21.

The composite layer of low k silicon oxide dielectric material further comprises a second layer 30 of low k silicon oxide dielectric material deposited over first layer 24 at a faster rate than the deposition rate of first layer 24 up to the desired overall thickness of the composite layer of low k carbon-doped silicon oxide dielectric material.	"A second layer of low k silicon oxide dielectric material, having a faster deposition rate than the first dielectric layer, is then deposited over the first layer up to the desired overall thickness of the low k silicon oxide dielectric layer." Page 6, lines 19-21.
The first layer of low k silicon oxide dielectric material may comprise a low k carbon-doped silicon oxide dielectric material formed by reacting a carbon-substituted silane reactant with hydrogen peroxide until the resulting deposition of low k carbon-substituted silicon oxide dielectric material reactant product reaches the level of the top of metal lines 14a-14c on oxide layer 10.	"Such void-free low k silicon oxide dielectric material may be deposited by reacting hydrogen peroxide with a carbon-substituted silane such as a methyl silane..." Page 8, lines 7–8.
The second layer of low k silicon oxide dielectric material may comprise a layer of low k carbon-doped silicon oxide dielectric material formed over the first layer by plasma enhanced chemical vapor deposition (PECVD) up to the desired overall thickness of the low k carbon-doped silicon oxide dielectric layer.	"...a second layer 30 of low k dielectric material is now deposited over the entire structure up to the desired thickness of the composite dielectric layer... in a PECVD process to deposit a low k silicon oxide dielectric layer." Page 9, lines 8-16.

(6) THE ISSUES

(i) Whether or not claims 15-16 and 18 are unpatentable under 35 U.S.C. 102(b) as being anticipated by Jeng U.S. Patent No. 5,821,621.

(ii) Whether or not claims 17 and 19 are unpatentable under 35 U.S.C. 102(b) as being anticipated by Jeng U.S. Patent No. 5,821,621.

(7) GROUPING OF CLAIMS BY ISSUES AND REJECTIONS

In accordance with the provisions of 37 CFR 1.192(c)(7), Applicants hereby state that claims 15-16 and 18 in group a below do not stand or fall together with claims 17 and 19 of group b below.

Group (a) The issue is whether or not Jeng U.S. Patent No. 5,821,621 anticipates the composite layer of low k silicon oxide dielectric materials as claimed by Applicants in claims 15-16, and 18.

Group (b) The issue is whether or not Jeng U.S. Patent No. 5,821,621 anticipates the composite layer of low k carbon-doped silicon oxide dielectric materials, including a first layer of low k carbon-doped silicon oxide dielectric material formed by reacting a carbon-substituted silane reactant with hydrogen peroxide as claimed by Applicants in claims 17 and 19.

(8) THE ARGUMENTS

(i) 35 U.S.C. 112, First Paragraph Issues — No Issues

(ii) 35 U.S.C. 112, Second Paragraph Issues — No Issues

(iii) 35 U.S.C. 102 Issues

(A) General Statement

Applicants' claimed invention, in all of Applicants' claims, includes a composite layer of two layers of low k silicon dielectric material. It is believed that the main disagreement between the Examiner and Applicants centers around whether or not Jeng's liner (22) reads on Applicants' first layer of low k silicon oxide dielectric material. It is not whether or not Jeng's layer (24) reads on Applicants' second layer of low k dielectric material.

(B) The Rejection of Claims 15-16 & 18* Under 35 U.S.C. 102(b) on Jeng U.S. Patent 5,821,621

(Jeng's liner layer 22 is neither "a low k silicon oxide "nor "a low k silicon oxide dielectric material exhibiting void-free deposition properties")

On page 2 of the first Office Action (mailed 01/31/2003), the Examiner states:

> "In re claims 15-16 & 18-19 Jeng discloses in fig.1-4 a composite layer of low k silicon oxide dielectric material (22) on an oxide layer (12) of an IC (fig. 1), said composite layer of low k silicon oxide dielectric material exhibiting void-free deposition properties (col. 4, lines 1-5) comprising: a first layer of low k ***silicon oxide*** dielectric material exhibiting ***void-free*** deposition properties (22); and a second layer of low k silicon oxide dielectric material (24) to a desired thickness." (emphasis added)

The above quoted portion of the 1st Office Action appears to be repeated verbatim in the Final Rejection. It has been Applicants' position that layer (22) is not identified by Jeng as either a low k silicon oxide dielectric material or as a low k silicon oxide dielectric material exhibiting void-free deposition properties in the passage cited by the Examiner (Jeng col. 4, lines 1-5). No other portion of Jeng has ever been subsequently identified by the Examiner as teaching that Jeng's layer (22) is a low k silicon oxide dielectric layer as recited in Applicants' claims. Neither has any other portion of Jeng ever been subsequently identified by the Examiner as teaching that Jeng's layer (22) is either a low k silicon oxide dielectric layer as recited in Applicants' claims or as a low k silicon oxide dielectric material exhibiting void-free deposition properties.

*The first grounds of rejection of Applicants' claims under 35 U.S.C. 102(b) on Jeng U.S. Patent 5,821,621 grouped together claims 15-16 and 18-19 as reciting: "...a low k silicon oxide dielectric material...", and claim 17 as reciting: "...a low k ***carbon-doped*** silicon oxide dielectric material...***formed by reacting a carbon-substituted silane reactant with hydrogen peroxide***" (emphasis added). Since both claims 17 and 19 recite the silicon oxide as "carbon doped" and *"formed by reacting a carbon-substituted silane reactant with hydrogen peroxide"*, Applicants have, therefore, grouped claim 19 with claim 17 rather than with claims 15-16 and 18.

Applicants have only found the following two passages in the Jeng patent which describe Jeng's liner layer 22. Neither of the passages supports the Examiners' position that Jeng's liner layer 22 is a low k silicon oxide dielectric layer, or that liner layer 22 is a low k silicon oxide dielectric material exhibiting void-free deposition properties. In the first of the two passages, Jeng states, at col. 4, lines 18-26:

> "Liner layer 22 is an optional layer to protect metal interconnect lines 14 from solvents used in some spin-on low-k materials to prevent oxidation of the metal interconnect lines. Liner layer 22 can be eliminated when non -interactive dielectric materials are used, that is dielectric materials that will react with the metal layer or materials used for the via contact. Liner layer 22 is typically a thin layer, 250Å-1,000Å coverage on blank wafer, of plasma enhanced TEOS with about 40% step coverage."

In the above first Jeng passage (col. 4, lines 18-26), Jeng identifies his liner layer 22 as a plasma enhanced TEOS. "TEOS" (tetraethyl orthosilicate) identifies the source of silicon, in the formation of the dielectric (tetraethyl orthosilicate). It is not synonymous with low k silicon oxide. This disclosure by Jeng does not teach or anticipate use of a low k silicon oxide dielectric material as required by Applicants' claims. Nor does it teach or anticipate the use of a low k silicon oxide dielectric material exhibiting void-free deposition properties, as also required by Applicants' claims.

In the second passage, Jeng states, at col. 4, lines 57-59:

> "The liner layer can be an etch stopping layer such as a low-dielectric organic spin-on-glass ***or*** silicon oxide." (emphasis added).

Note that Jeng does NOT state here that liner 22 is a low k silicon oxide dielectric material! Rather he states that liner 22 may be a low-dielectric spin-on-glass OR it may be silicon oxide. Jeng does not anticipate the use of a low k silicon oxide dielectric material for liner 22 in this passage either. Again, Applicants' claimed invention is not taught by Jeng.

(C) The Rejection of Claims 17 & 19 Under 35 U.S.C. 102(b) on Jeng U.S. Patent 5,821,621

(Jeng's liner layer 22 does not anticipate a "low k carbon-doped silicon oxide " nor does it anticipate "a low k silicon oxide dielectric material formed reacting a carbon-substituted silane reactant with hydrogen peroxide")

The first Office Action, in rejecting claim 17, states:

> "Jeng discloses a composite layer of low k carbon doped silicon oxide (22, col. 1 lines 45-55, table in col. 5) exhibiting void-free deposition properties, comprising: a first layer of low k carbon-doped silicon oxide dielectric (22); and a second layer of carbon-doped low k silicon oxide (24) by PECVD (col.4 lines 63-65)."

Totally ignored by the Examiner is the limitation "...formed by reacting a carbon-substituted silane reactant with hydrogen peroxide ..." (found in claim 17 at lines 6-7, or the similar limitation found in claim 19 at lines 7-9).

The portion of the Jeng patent cited by the Examiner in support of her position that Jeng allegedly teaches a composite layer of low k carbon-doped silicon oxide is col. 1, lines 45-55, which reads as follows:

> "As used herein, low dielectric constant or low-k means a material having a dielectric constant of lower than 4 and preferably lower than 3 and most preferably about 2 or lower. Unfortunately materials having a lower dielectric constant have characteristics that make them difficult to integrate into existing integrated circuit structures and processes. Many polymeric materials such as polysilsquioxane, parylene, polyimide, benzocyclobutene, and amorphous TEFLON have lower dielectric constants (lower permitivities). Other preferred materials are Aerogel, or Xerogel which are typically made from a gelation of tetraethyl orthosilicate stock solution."

There is nothing in this Jeng passage, however, which refers to the composition of Jeng's layer 22. Rather the passage merely refers to low k dielectric materials in general which is followed by a passage (not cited by the Examiner) explaining the shortcomings of such materials and why the use of such materials as a stand alone replacement for SiO_2 is very difficult if not impossible. Jeng may be referring to his choice of dielectric materials for layer (24). Furthermore, Jeng contains no

teachings regarding the limitation in Applicants' claims 17 and 19 "...formed by reacting a carbon-substituted silane reactant with hydrogen peroxide ...".

It should be further noted that the initial Rejection also refers to Table 5 in Jeng. However, Applicants and the Examiner now agree that Table 5 is irrelevant to the claimed invention (see page 7, lines 7-15 of Applicants' amendment dated 4/2/2003, and page 3, lines 13-15 of the Final Rejection).

Claims 17 and 19 are not anticipated by Jeng. Claim 17 (and claim 19) are patentable over the Jeng reference.

(iv) Section 103 Issues — No Issues

(v) Miscellaneous Additional Issues in the Final Rejection of Claims 15-19

(A) Examiner's Five Reasons Why Appellants' Arguments Are Moot

In the Final Rejection, Appellants' claims 15-19 were again rejected under 35 U.S.C. § 102(b) as being anticipated by Jeng U.S. Patent 5,821,621. Appellants, in their previous response, argued that Jeng did not teach that his liner layer (22), used to inhibit interaction between his metal lines (14) and his dielectric materials, was a low k silicon oxide dielectric material.

The Final Rejection acknowledged (and rejected) Appellants' arguments that they had been unable to find where Jeng taught that his liner layer (22), used to inhibit interaction between his metal lines (14), comprised a low k silicon oxide material. The Examiner stated that Appellants' point was moot for the following five reasons:

(1) The instant claims fail to claim the dielectric constant or properties associated with a low k dielectric;

(2) Jeng discloses in figures 1-4 a low k silicon oxide dielectric layer (22);

(3) It is well known in the art that silicon oxide is a low k dielectric;

(4) The dielectric constant of silicon oxide is 3.8-4.2 which is considered low k dielectric material (see Nalwa, Handbook of Low and High Dielectric Constant Materials and Their Applications, Vol. 1, pg. 66 (1999)); and

(5) Jeng teaches that low k means a dielectric lower than 4.0. Therefore, since the method of Jeng teaches silicon oxide as the first layer, Jeng is inherently teaching low k dielectric because the values of the dielectric constant for silicon oxide are inherent to be in the art recognized range of lower than 4.0.

(1) The Alleged Failure to Claim the Dielectric Constant

With respect to the USPTO's first reason why arguing that liner layer (22) is not a low k dielectric material is a moot point, each of Appellants' claims recite a ***low k*** first layer and a ***low k*** second layer. Further more, the term "low k" is defined in Appellants' specification on page 6, lines 22-24.

The courts have long held that the specification may be used in the interpretation of what claim terminology means. For example, the CAFC, in McGill Inc. v. John Zink Co., 221 U.S.P.Q. 944, stated, at pages 949-950:

> "Another factor in claim construction is the use of the patent specification. McClain v. Ortmayer, 141 U.S. 419 (1891); Fromson, 720 F.2nd at 1569-70, 219 USPQ at 1140. Words which were defined in the specification must be given the same meaning when used in a claim. General Electric Co. v. United States, 572 F.2nd 745, 753, 198 USPQ 65, 71 (Ct. Cl. 1978). In Autogiro, 348 F.2nd at 397-98, 155 USPQ at 702-3, the Court of claims stated:
>
> > 'In serving its statutory purpose, the specification aids in ascertaining the scope and meaning of the language employed in the claims inasmuch as words must be used in the same way in both the claims and the specification. U.S.Pat.Off. Rule 75(d). The use of the specification as a concordance for the claims is accepted by almost every court, and is a basic concept of patent law.'"

Appellants' arguments are not moot for this reason.

(2) The Alleged Disclosure of Low K Silicon Oxide Dielectric in Jeng's Figures 1-4

The second reason is alleged to be that Jeng discloses in figs. 1-4 a low k silicon oxide dielectric layer (22). Jeng's figs. 1-4 contain no labels or other identifying words on any of the first four figures. The figures, taken alone, disclose nothing with respect to the dielectric constant of the material used to construct liner 22. Therefore, one must refer back to the Jeng specification to find any identification of liner layer (22). The deficiencies of Jeng's specification on this point have been discussed above.

(3) The Allegation That It Is Common Knowledge That SiO_2 Is a Low K Dielectric Material

The third point of the USPTO is that it is well known in the art that silicon oxide is a low k dielectric material. Appellants respectfully request that the Examiner provide some proof of this allegation. Should the Examiner find such evidence that silicon oxide (per se) is well known (in the integrated circuit field) as a low k dielectric material, it is believed that many skilled in the art will be very shocked to learn this. Included in that group will be Jeng himself, since he makes it clear at col. 1, lines 41-45, that he does not regard SiO_2 to be a low k silicon oxide dielectric material.

(4) The Allegation That a Dielectric Constant, Ranging from 3.8-4.2 for Silicon Oxide, is Considered to Be a Low K Dielectric

The Examiner introduces a table from a new reference at this point in the prosecution (i.e., in the Final Rejection, in apparent violation of MPEP 706.07(a), since Appellants did not amend their claims subsequent to issuance of the first Office Action).

The new reference comprises a table apparently found on page 66 of a handbook by Nalwa. This table, entitled "Summary of Properties of Materials Described", lists the dielectric constant of silicon ranging from 3.8 to 4.2. Appellants are confused as to what such data is intended to prove. Of the dielectric constants listed for 29 materials, only boron nitride has a higher dielectric constant value.

How this supports a contention that conventional silicon oxide is a low k dielectric material is not apparent. (Note in this regard that the mere listing of silicon oxide with materials having lower dielectric properties does not make silicon oxide a low k dielectric material.)

It is noted that the title of the Nalwa handbook reads "Handbook of Low ***and High*** Dielectric Constant Materials...". (emphasis added) Perhaps the inclusion of silicon oxide, in the table on page 66 of the handbook reference, was to furnish an example of a high dielectric material.

The citation of the Nalwa reference in the Final Rejection is not only untimely, but is also improper as an additional reference in a Section 102 rejection. It is hornbook law that for a claim to be anticipated by a reference under Section 102, ***all*** the elements in the claim must be shown in a ***single*** reference. The CAFC, in Connell v. Sears Roebuck & Co., 220 USPQ 193, stated, at page 198:

> "Anticipation requires the presence in a ***single*** prior art disclosure of all elements of a claimed invention arranged as in the claim." (emphasis added)

The same court repeated this requirement in W.L. Gore & Associates, Inc. v. Garlock, Inc., 220 USPQ 303, at page 313 and in Carman Industries, Inc. v. Wahl, 220 USPQ 481, where it stated, at page 485:

> "Lacking an element of the claims, the reference cannot anticipate them under section 102."

There are no teachings in either Jeng or Nalwa that a dielectric constant range of 3.8-4.2 for silicon oxide is considered to be a low k dielectric material.

(5) The Allegation that Jeng Teaches the Use of Silicon Oxide as a Low K Dielectric Material for Liner Layer 22

The Examiner, in her Final Rejection of Appellants' claims, states that: "Jeng teaches that low k means a dielectric lower than 4.0." She goes on to say: "Therefore, the method of Jeng teaches silicon oxide as the first layer, which is inherently teaching low k dielectric because the values of the

dielectric constant for silicon oxide are inherent to be in the art recognized range of lower than 4.0." (emphasis in original)

The problem with this allegation (as understood) is that it appears to require the Jeng reference to contradict itself. In col. 1, lines 40-41, Jeng clearly states: "The intermetal dielectric (IMD) of the prior art is typically SiO_2 ***which has a dielectric constant of about 4.0*** ." (emphasis added) Therefore, when Jeng teaches silicon oxide as the first layer (as conceded by the Examiner), Jeng is ***not*** teaching the use of a low k material for the first layer because Jeng explicitly states that SiO_2 has a dielectric constant of about 4.0, and just as explicitly states: "As used herein, low dielectric constant or low-k means a material having a dielectric constant of ***lower than 4***..." (emphasis added). In other words Jeng is teaching that a low k dielectric material means a dielectric material having a dielectric constant lower than silicon oxide. Therefore, when Jeng uses silicon oxide for the first layer, Jeng is not using low k dielectric material. It should be further noted that inherency is used as a substitute when an actual value or property is absent. This is not the case here. Jeng has been very specific about the respective dielectric constants of SiO_2 and low k silicon oxide dielectric material.

(B) Miscellaneous Comments Regarding Patentability of Appellants Claims

(1) Void-Free First Layer of Low K Silicon Oxide Dielectric Material

Appellants' independent claims 15 and 17-19 , in part a), all recite that the first layer is further characterized as a void-free low k silicon oxide dielectric material. No such teaching is found in Jeng, despite the requirements for a section 102 rejection.

(2) First Layer of Low K Silicon Oxide Dielectric Material Made from Specific Reactants to Form Void-free Silicon Oxide Dielectric Material

Appellants' claims 17 and 19 further recite specific reactants which, when reacted together, will not merely form a low k silicon oxide dielectric material, but will form void-free low k silicon oxide dielectric material between the metal lines.

(3) Planarized First Layer of Low K Silicon Oxide Dielectric Material

Claims 18 and 19 both recite that the first layer of low k silicon oxide dielectric material is planarized before formation of the second low k layer of silicon oxide dielectric material is formed thereon. As discussed in Appellants' specification at page 11, line 23 to page 12, line 2, this planarization step is preferable when it is desirable to form vias down to the metal lines without contacting the void-free low k silicon oxide dielectric material in the first low k silicon oxide dielectric layer.

(C) Examiner's Response in Advisory Action Appears to Introduce a New Rejection

The Examiner admits, in the Advisory Action (mailed to the Appellants within 16 days of the end of the six months statutory period for response despite Appellants' prompt two months reply to the Final Rejection), that Jeng does not teach that silicon oxide has a dielectric constant of less than 4.0. Then she states that the Nalwa reference teaches that the dielectric constant of silicon oxide is about 3.8 to 4.2. Then, apparently in an attempt to salvage something from her rejection, she makes the statement:

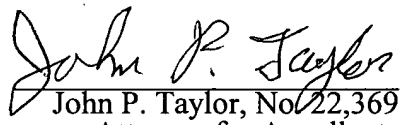
> "Therefore, it would have been ***obvious*** to one skilled in the art at the time of the invention to ***modify*** the process of Jeng to use a silicon oxide layer with a dielectric constant less than 4.0 in order to form a low k dielectric layer." (emphasis added).

Although the Examiner now unseasonably introduces a Section 103 into the case, Appellants will respond by stating that there is nothing in this combination of references to suggest that Jeng's layer 22 should comprise a low k silicon oxide dielectric material characterized as void-free.

(vi) Conclusion

Jeng U.S. Patent 5,821,621does not teach or anticipate Appellants' claimed composite of low k silicon oxide material comprising a first layer of low k silicon oxide dielectric material exhibiting void-free deposition characteristics, and a second layer of low k silicon oxide dielectric material capable of depositing at a higher rate than the void-free lower layer. Jeng only teaches a single layer of low k dielectric material (24) over which Jeng forms a layer of standard k dielectric material (28) Appellants' claimed structure is patentable over the references.

Respectfully Submitted,



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(9) APPENDIX A

(CLAIMS ON APPEAL)

15. A composite layer of low k silicon oxide dielectric material on an oxide layer of an integrated circuit structure, said composite layer of low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions, deposition rates in other regions comparable to standard k silicon oxide, and without exhibiting via poisoning characteristics, comprising:

a) a first layer of low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions, deposited until said low k silicon oxide dielectric material reaches the level of the top of metal lines on said oxide layer; and

b) a second layer of low k silicon oxide dielectric material deposited over the first layer at a faster rate than the deposition rate of said first layer up to the desired overall thickness of the composite layer of low k carbon-doped silicon oxide dielectric material.

16. The composite layer of low k silicon oxide dielectric material of claim 15 wherein said first and second layers comprising said composite layer of low k silicon oxide dielectric material are all formed in a single vacuum processing apparatus without removal of said semiconductor substrate from said vacuum apparatus.

17. A composite layer of low k carbon-doped silicon oxide dielectric material on an oxide layer of an integrated circuit structure on a semiconductor substrate, said composite layer of low k carbon-doped silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions, deposition rates comparable to non carbon-doped silicon oxide, and without exhibiting via poisoning characteristics, comprising:

a) a first layer of low k carbon-doped silicon oxide dielectric material formed by reacting a carbon-substituted silane reactant with hydrogen peroxide until the resulting deposition of low k carbon-doped silicon oxide dielectric material reaction product reaches the level of the top of metal lines on the oxide layer; and

b) a second layer of carbon-doped low k silicon oxide dielectric material formed over said first layer by plasma enhanced chemical vapor deposition (PECVD) up to the desired overall thickness of the low k carbon-doped silicon oxide dielectric layer.

18. A composite layer of low k silicon oxide dielectric material on an oxide layer of an integrated circuit structure on a semiconductor substrate having closely spaced apart metal lines thereon, said composite layer of low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions between closely spaced apart metal lines, deposition rates in other regions comparable to standard k silicon oxide, and without exhibiting via poisoning characteristics, and said composite layer further comprising:

a) a first layer of low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions between said closely spaced apart metal lines, said first layer of low k silicon oxide dielectric material formed over said oxide layer and said metal lines up to at least the level of the top of said metal lines on said oxide layer and planarized down to said top of said metal lines; and

b) a second layer of low k silicon oxide dielectric material over said planarized first layer and said top of said metal lines, said second layer of low k silicon oxide dielectric material deposited at a higher deposition rate than said first low k layer.

19. A composite layer of low k carbon-doped silicon oxide dielectric material on an oxide layer of an integrated circuit structure on a semiconductor substrate, said composite layer of low k carbon-doped silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions between closely spaced apart metal lines, deposition rates comparable to non carbon-doped silicon oxide, and without exhibiting via poisoning characteristics, said composite layer further comprising:

a) a first layer of low k carbon-doped silicon oxide dielectric material formed over said oxide layer and said metal lines by reacting a carbon-substituted silane reactant with hydrogen peroxide until the resulting deposition of low k carbon-doped silicon oxide dielectric material reaction product reaches at least the level of the top of said metal lines on the oxide layer to form a low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions between said closely spaced apart metal lines, said first layer of low k silicon oxide dielectric. material planarized down to said top of said metal lines; and

b) a second layer of carbon-doped low k silicon oxide dielectric material formed over said planarized first layer and over said tops of said metal lines up to the desired overall thickness of the low k carbon-doped silicon oxide dielectric layer by plasma enhanced chemical vapor deposition (PECVD), said second layer of low k silicon oxide dielectric material deposited at a higher deposition rate than said first layer.

APPENDIX B

(REFERENCES APPLIED AGAINST APPELLANTS' CLAIMS)

A. Jeng U.S. Patent 5,821,621

Jeng U.S. Patent 5,821,621 discloses an improved method for integrating polymer and other low dielectric constant materials, which may have undesirable physical properties, into integrated circuit structures and processes, especially those requiring multiple levels of interconnect lines. Jeng combines the advantages of SiO_2 dielectric material with low dielectric constant materials by placing the low dielectric material only between tightly spaced apart lines. The inventor discusses the various types of undesirable capacitance which occur in integrated circuit structures, such as line to line capacitance and line to ground capacitance, and concludes that of those two types of capacitance, more than 90% is line to line capacitance. Jeng states that many polymeric materials have low dielectric constants, but also have a number of shortcomings with respect to at least their physical properties.

Jeng proposes to take advantage of the desirable low k characteristics of such polymeric dielectric materials by using this low k dielectric material only between closely spaced apart metal lines. Jeng does so by first applying a thin liner layer (22) over the metal lines (14) and then spinning a low-k dielectric material across the surface of the wafer to fill the critical areas (24), i.e., the areas between closely spaced together interconnect lines. This also serves to fill all of the areas between all interconnect lines, i.e., the non-critical areas as well. The areas where the low-k material is to remain, are masked off with a resist mask. The unmasked low dielectric constant material in non-critical or widely spaced areas is then etched away, leaving the problematic but desirable low-k material in only those areas where needed, e.g., between closely spaced apart interconnect lines.

After removal of the resist mask, a layer of conventional dielectric material (28), such as SiO_2, is applied over the entire structure, including the etched away areas, to fill the remaining area with SiO_2, e.g., to provide spacing between more widely spaced apart metal lines.

B. Nalwa, Handbook of Low and High Dielectric Constant Materials and Their Applications, Vol. 1, pg. 66 (1999)

Page 66 of the Nalwa Handbook comprises Table XIV entitled "Summary of Properties of Materials Described". This table lists various properties of a number of materials, including (according to the Examiner) their dielectric constants.